Gold Nanoparticles Floating Gate MISFET for Non-Volatile Memory Applications

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OUTLINE

• Objectives and main target
• Fabrication technology
• Electrical Measurements
• Conclusions
TARGET

- Longer term objective: Realize a flash-type memory device at low temperature (<400°C) from c-Si for possible application in 3-D architecture.
- A critical first step is the realization of memory nodes at low temperature over a conventional (high temperature) Si device.
- Gold nanoparticles, deposited at room temperature, were chosen as the charge storage elements.
Approach:
‘Integrate’ gold nanoparticles deposited at room temperature into a silicon device

Crystalline Si
Metal gate
Fabrication Process

Silicon infrastructure where the nanoparticles will be deposited

1. A resist is used as a mask for S/D As implant
2. A TEOS SiO₂ film is deposited and the channel opened
3. Source/Drain metal contacts are formed

SOI wafer

Si channel

Represents the area that has been protected with resist (non-doped with As area)
Fabrication Process:

I. Formation of conventional Si MOSFET

1) 10 nm sacrificial thermal oxide
2) Definition of the Device area using RIE
3) Formation of Source (S) and Drain (D) by As ion implantation: $2 \times 10^{15} \text{ cm}^{-2}$, 60 KeV
4) Boron implantation for threshold voltage adjustment: $5 \times 10^{12} \text{ cm}^{-2}$, 30 KeV
5) Annealing at 950 °C for 30 min
6) Deposition of 100 nm TEOS oxide
7) Window opening down to Si at the Channel area
8) Formation of 5nm thermal gate oxide
9) S / D Al pads formation
Conventional Transistor structure

SEM image of an overview of the MOS transistor layout. In the inset the channel area (WxL) is shown.
Hybrid Transistor structure

To fabricate a memory transistor a stack of insulators and nanoparticles is then deposited.

Crystalline Si

Metal gate

Organic Insulator

Gold nanoparticles

SiO₂

Silicon

Aluminum

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Memory Stack

- **SiO$_2$:** Thermal oxide 5 nm
- **Gold nanoparticles:** SiO$_2$ functionalization and nanoparticle attachement
- **Organic Insulator:** Langmuir-Blodgett Cadmium Arachidate film (54 nm)

Aluminum  
Silicon  
Organic Insulator  
Gold nanoparticles  
SiO$_2$
Two ‘gold nanoparticle deposition technologies’ used and tested on MOS transistors

• Gold nanoparticles deposited through chemical self-assembly and SiO₂ surface functionalisation
• Gold nanoparticles deposited by LB technique
TEM and AFM images of Au nanoparticles deposited by chemical processing (Univ. of Durham)
Al Gate metallization

- Classical metallization process has been modified to avoid damaging the LB deposited films
- Capacitor structures and Transistors have been fabricated and measured
Metallization process

• During the Al evaporation a relatively low deposition rate was used to avoid heating the wafer.
• For gate electrode patterning, AZ5214 photoresist was used.
• After resist spinning a pre-bake step was performed at $T=65^\circ\text{C}$ for 60 min. The photoresist was patterned followed by a post-bake step at $65^\circ\text{C}$ for 90 min on a hot-plate.
• Aluminum etching was performed by dipping the samples into AZ726 developer for 90 sec at room temperature.
Metallization results

- Capacitors

- FET

- Chip with FETs
Electrical Characterization of memory devices

Comparative Id-Vg curves

Reference (SiO₂ insulator)
- - - - - Insulator Stack (LB/SiO₂ insulators)
- - - - - Memory Stack (LB/Au-nps/SiO₂ )
MISFET with embedded Au nano-particles into the gate insulator tested with different voltage sweep limits: (open circles) ±2V, (solid line) ±4V
Write/Erase (W/E) process obtained by applying ±6V voltage pulses respectively. The pulse period was 1s.

The effect of the programming voltage on the memory window for pulse 1s.
Retention characteristics of the device after application of ±6 V on the gate for 1 sec.
LB deposited gold nanoparticles

Voltage pulse: ±8V
Pulse width: 1s

CLEAR MEMORY EFFECT!
Conclusions and next steps

⇒ We have demonstrated a hybrid silicon-“chemical” technologies for room temperature formation of gold nanoparticles

⇒ Both Gold nanoparticle deposition technologies give nice memory device properties

⇒ One problem is the charging of the nanoparticles from the gate.

⇒ Solution: Use thinner SiO$_2$ layers (3 nm) and thicker organic insulator

or change the organic insulator with a deposited SiO$_2$ layer